WHAT IS CLAIMED IS:

1. A method of making an isolation-less array of non-volatile memory cells in a semiconductor substrate, having a planar surface; said substrate is of a first conductively type comprising;

forming a plurality of spaced apart trenches in said planar surface of said substrate in a first direction, each trench having a first sidewall, a second sidewall and a bottom wall;

forming a pair of floating gates along the first and second sidewalls in each trench, each floating gate spaced apart from the first and second sidewalls, respectively;

forming a first terminal of a second conductivity type along the bottom wall of each trench in the substrate;

forming a control gate in each trench; each control gate insulated from and capacitively coupled to the floating gates in the trench and insulated from the first terminal along the bottom wall of the trench;

forming a conductor on said planar surface, said conductor spaced apart from said planar surface;

patterning said conductor along a second direction substantially perpendicular to said first direction to form a plurality of spaced apart strips of conductors, with an opening between each paid of conductor strips; and

cutting each pair of floating gates in each trench.

2. The method of claim 1 wherein the step of forming a pair of floating gates comprises:

forming a layer of silicon dioxide along said first sidewall, said second sidewall, and said bottom wall of each trench;

depositing a layer of polysilicon along said silicon dioxide of said first sidewall, said second sidewall and said bottom wall of each trench;

anisotropically etching said layer of polysilicon, to remove said layer of polysilicon from said bottom wall, forming a pair of polysilicon floating gate spacers along the first and second sidewalls in each trench.

3. The method of claim 2 further comprising the step of forming a tip along each of said floating gates at an end closest to said bottom wall in each trench.

4. The method of claim 2 further comprising the step of forming a tip along each of said floating gates at an end furthest away from said bottom wall in each trench.

5. The method of claim 1 wherein said cutting step cuts each pair of floating gates through said opening in each trench without cutting the control gate.

6. The method of claim 2, wherein said step of forming a plurality of spaced apart trenches in said planar surface further comprises:

applying a layer of masking material on said planar surface of said substrate;

patterning said masking material in said first direction to form a plurality of masking strips and a plurality of first openings with a first opening between each pair of masking strips;

etching said substrate to form said plurality of trenches through said first openings.

7. The method of claim 6 wherein the masking material is silicon nitride.

8. The method of claim 1 wherein said cutting step is performed prior to said control gate being formed in each trench.

9. The method of claim 8 wherein the step of forming a pair of floating gates comprises:

forming a layer of silicon dioxide along said first sidewall, said second sidewall, and said bottom wall of each trench;

depositing a layer of polysilicon along said silicon dioxide of said first sidewall, said second sidewall and said bottom wall of each trench;

anisotropically etching said layer of polysilicon, to remove said layer of polysilicon from said bottom wall, forming a pair of polysilicon floating gate spacers along the first and second sidewalls in each trench.

10. The method of claim 9 further comprising the step of forming a tip along each of said floating gates at an end closest to said bottom wall in each trench.

11. The method of claim 9 further comprising the step of forming a tip along each of said floating gates at an end furthest away from said bottom wall in each trench.